

100 →

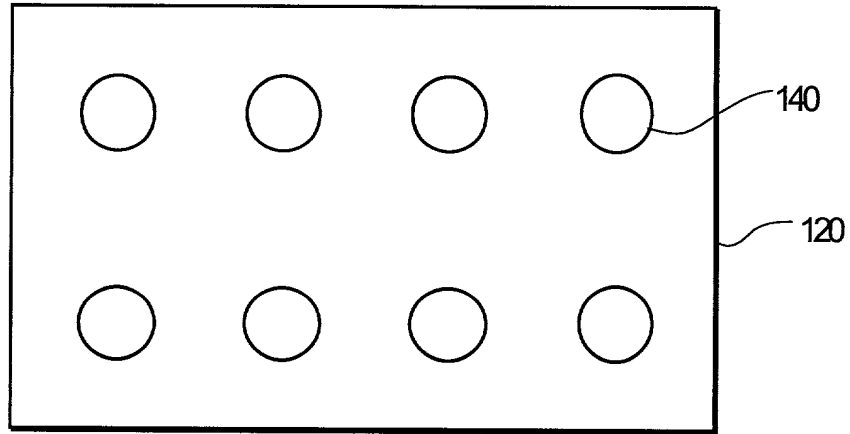


FIG. 1A
(PRIOR ART)

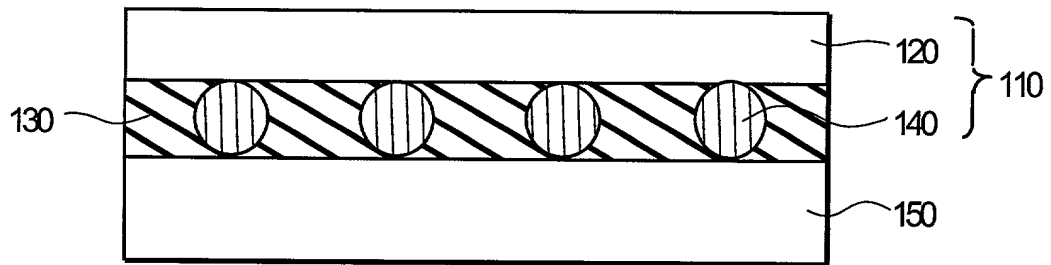


FIG. 1B
(PRIOR ART)

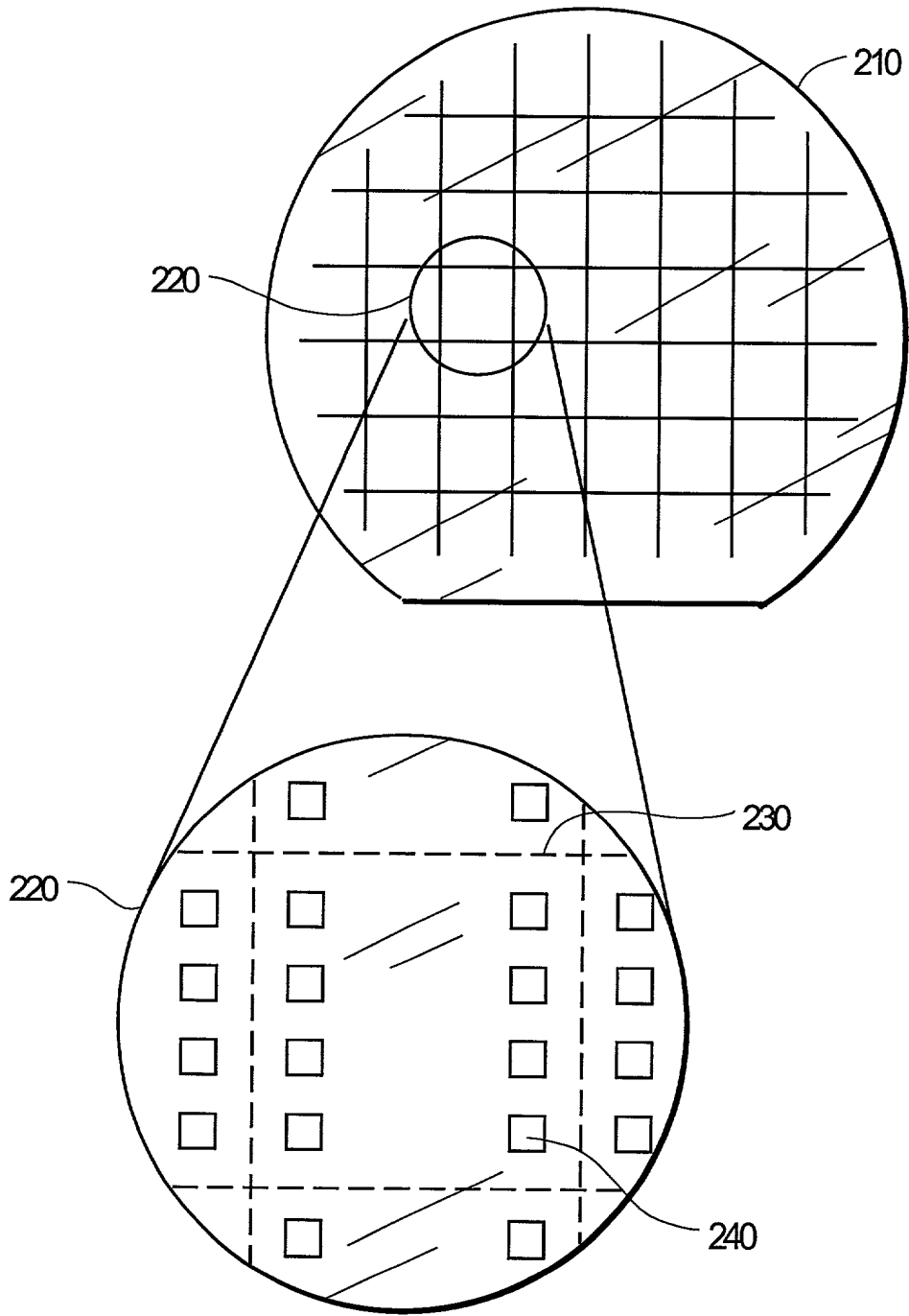


FIG. 2

FIG. 3A is a schematic diagram of a device 300 in a perspective view. The device 300 includes a substrate 310 and a plurality of conductive traces 320. The conductive traces 320 are arranged in a grid pattern on the substrate 310. The device 300 is shown in a perspective view, with the substrate 310 and the conductive traces 320 being clearly visible.

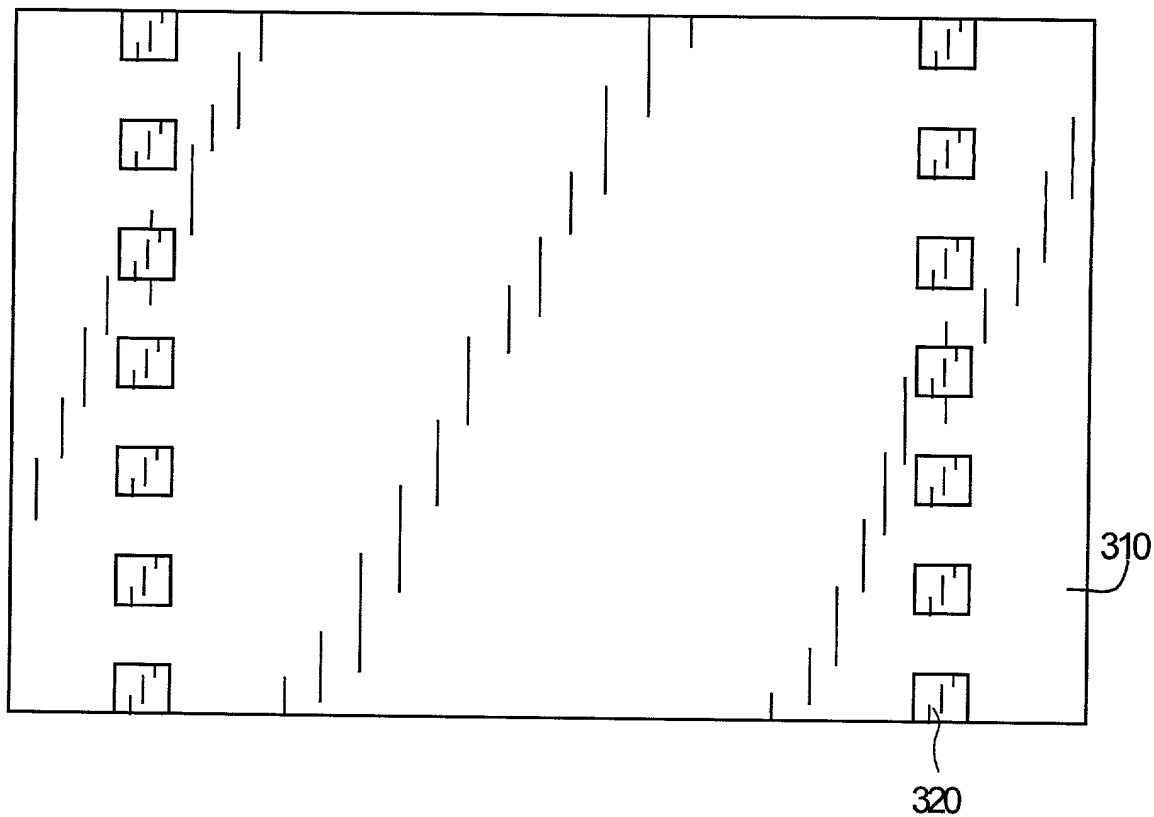


FIG. 3A

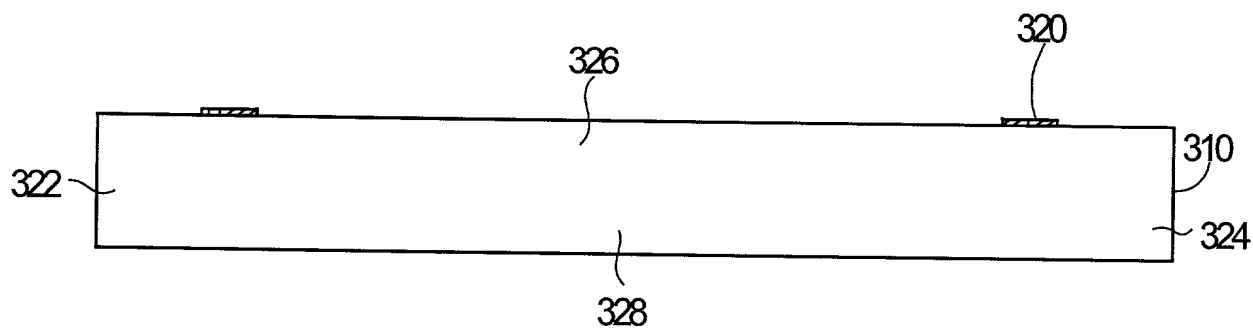


FIG. 3B

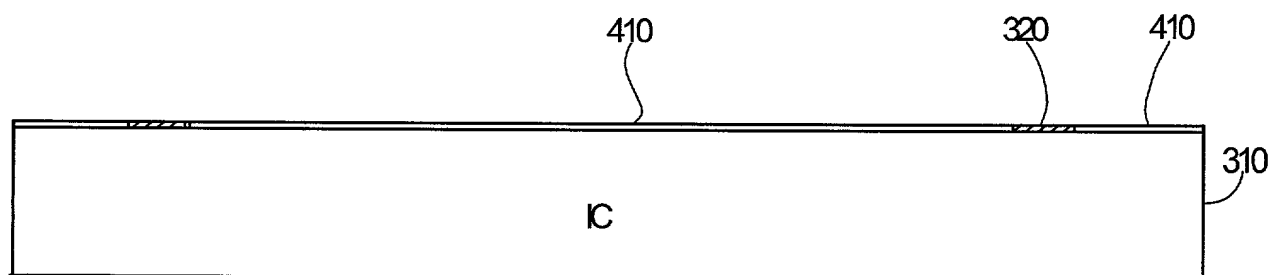
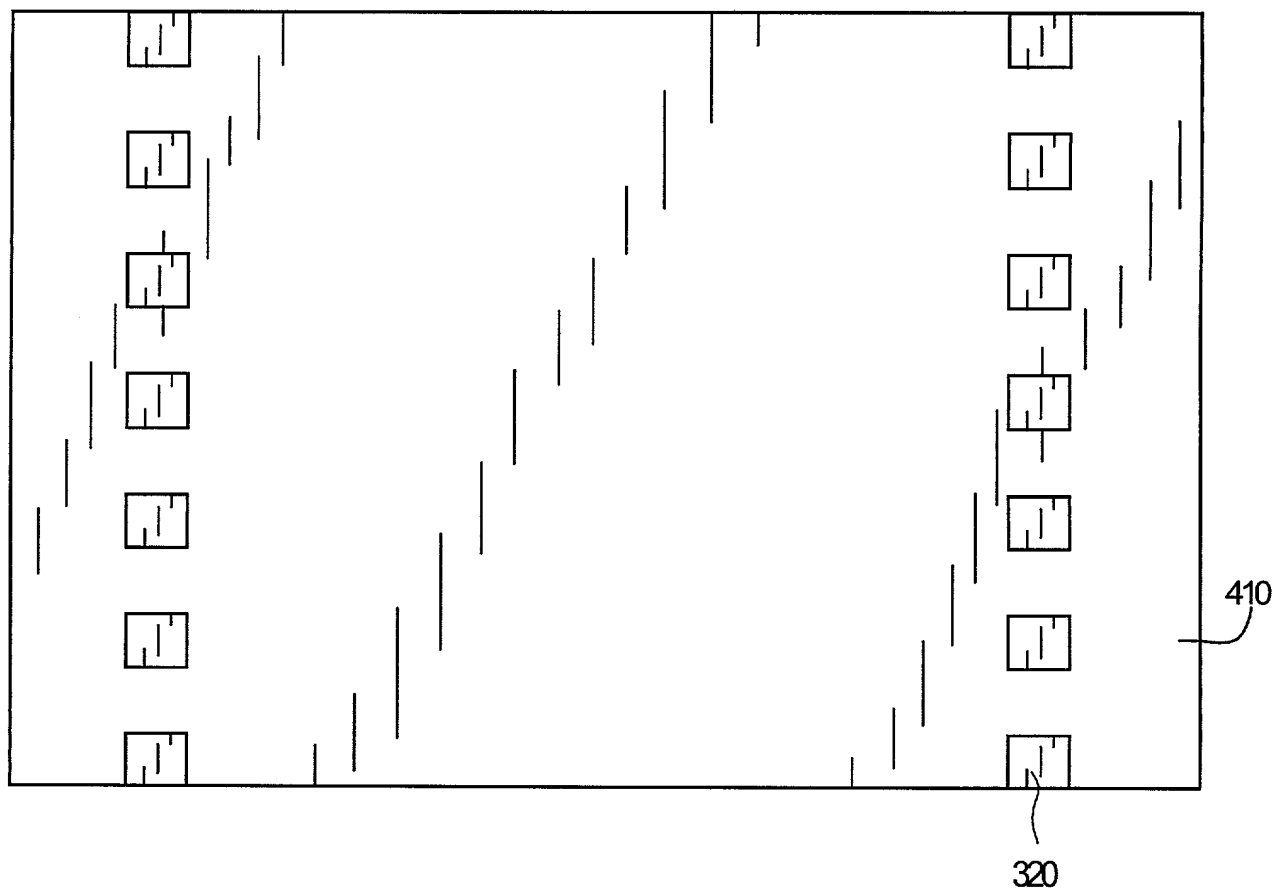


FIG. 5A is a schematic diagram of a device 500 in a first state. The device 500 includes a substrate 510 and a plurality of conductive traces 410. The conductive traces 410 are arranged in a grid pattern on the substrate 510. The device 500 is shown in a perspective view.

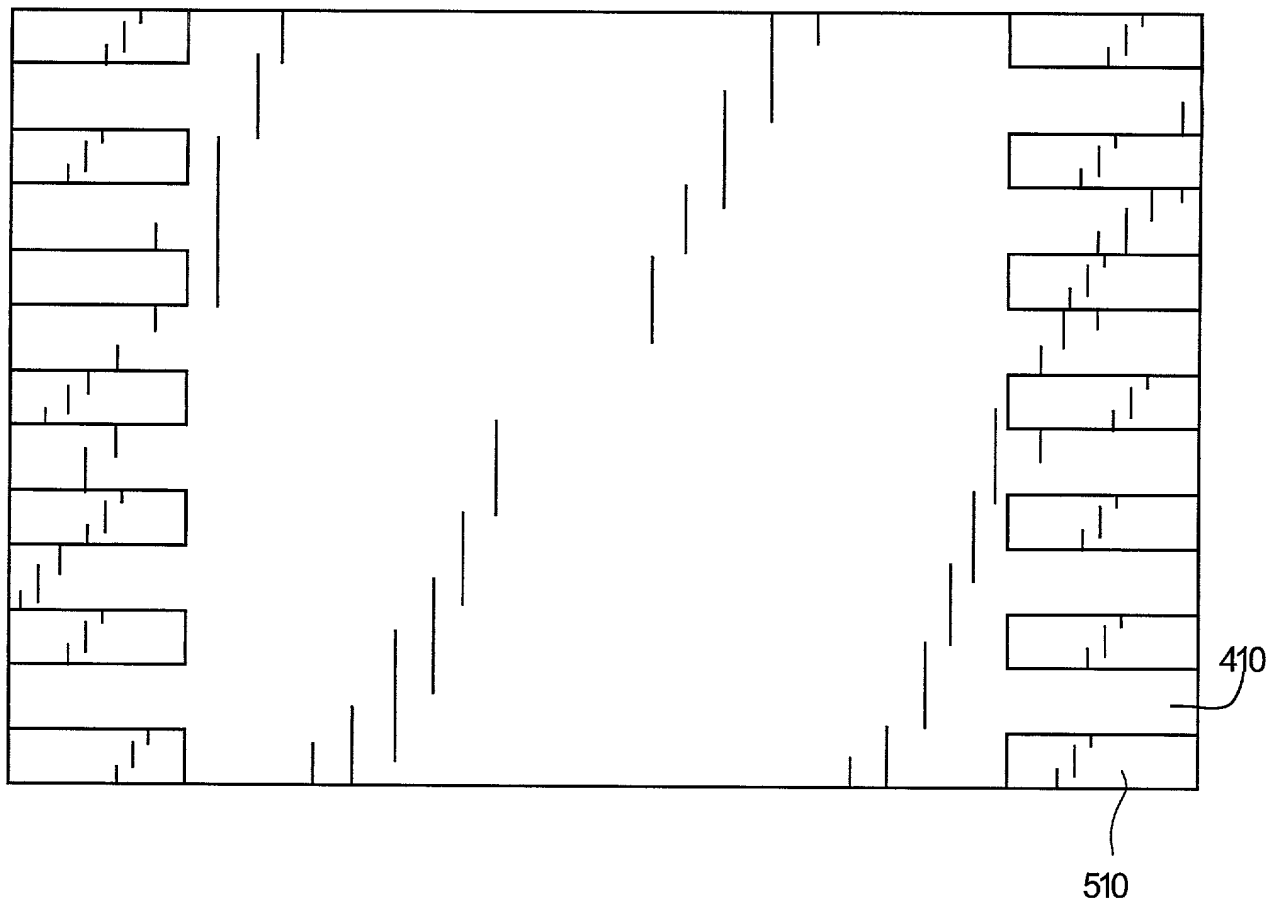


FIG. 5A

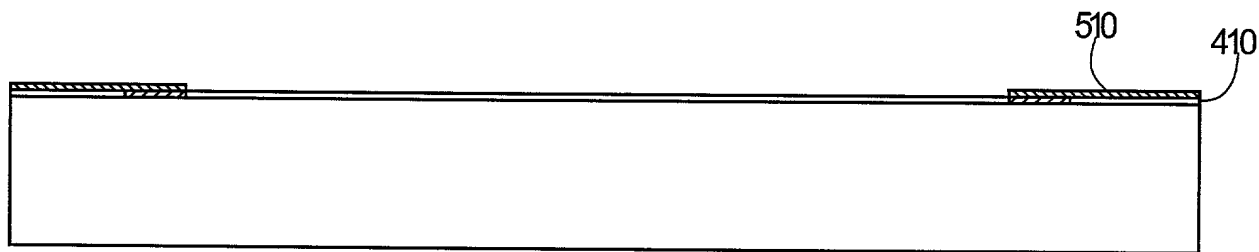
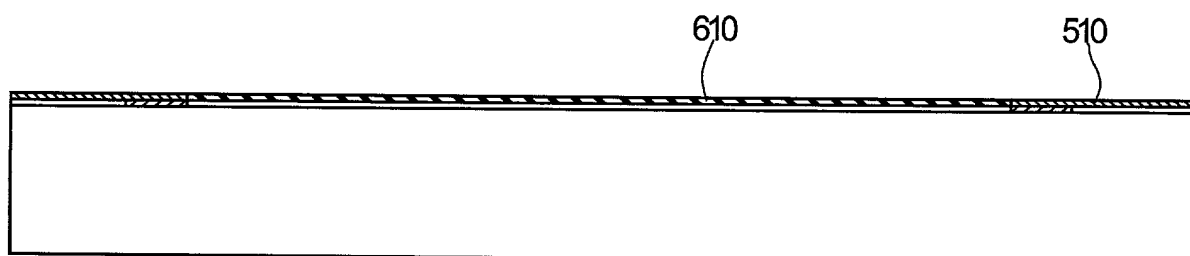
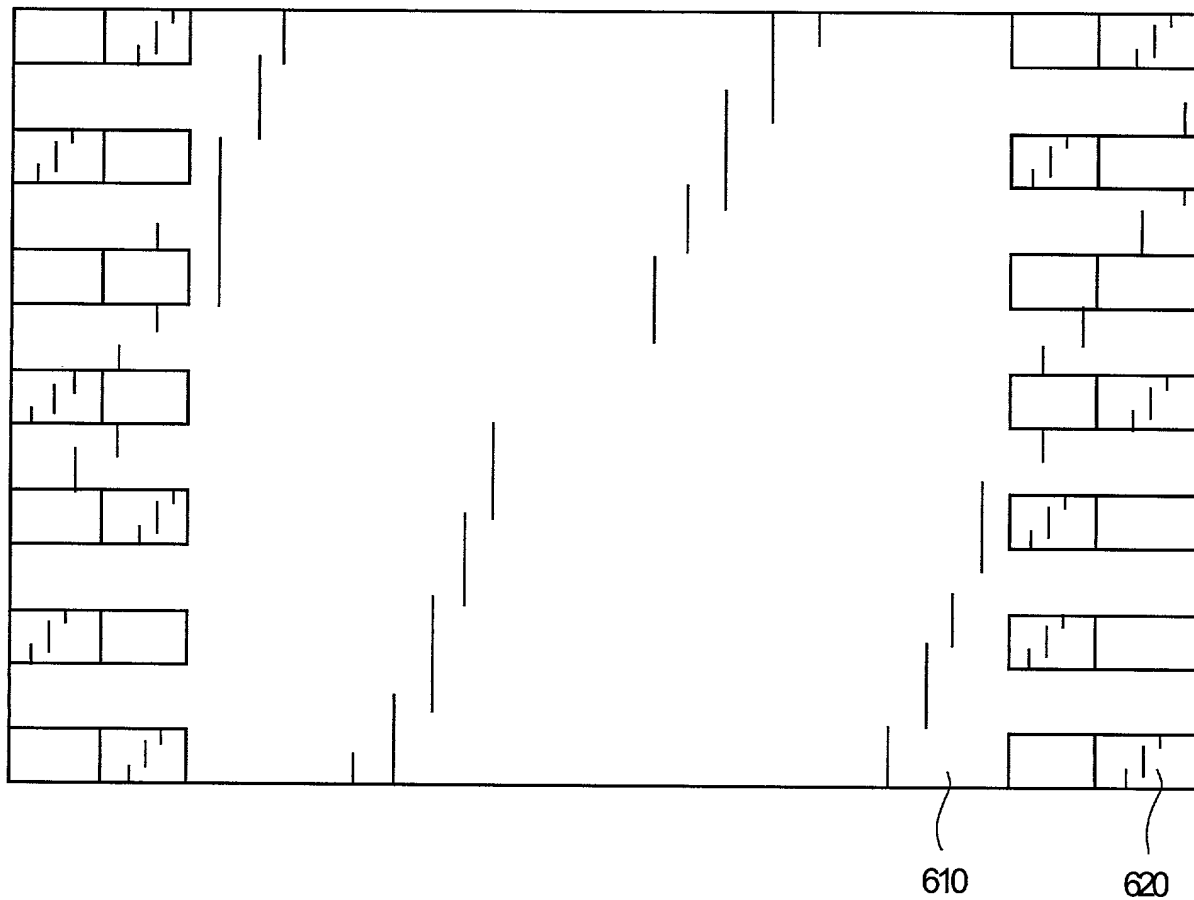
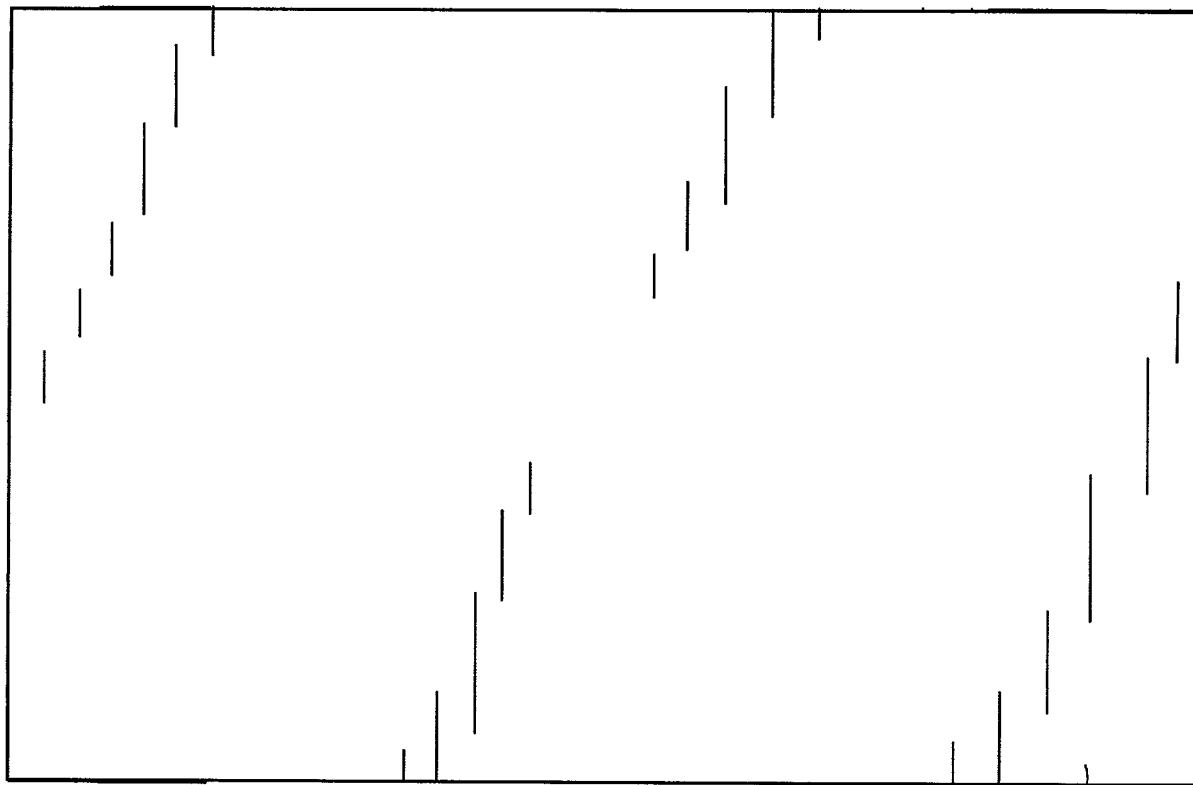


FIG. 5B





710

FIG. 7A

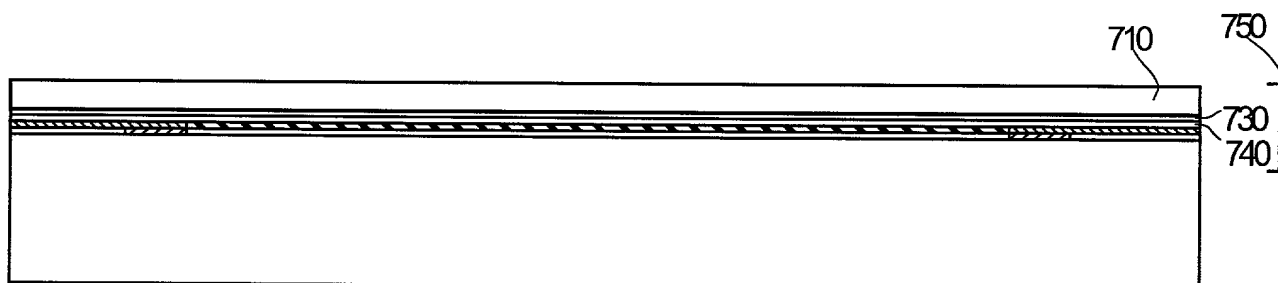
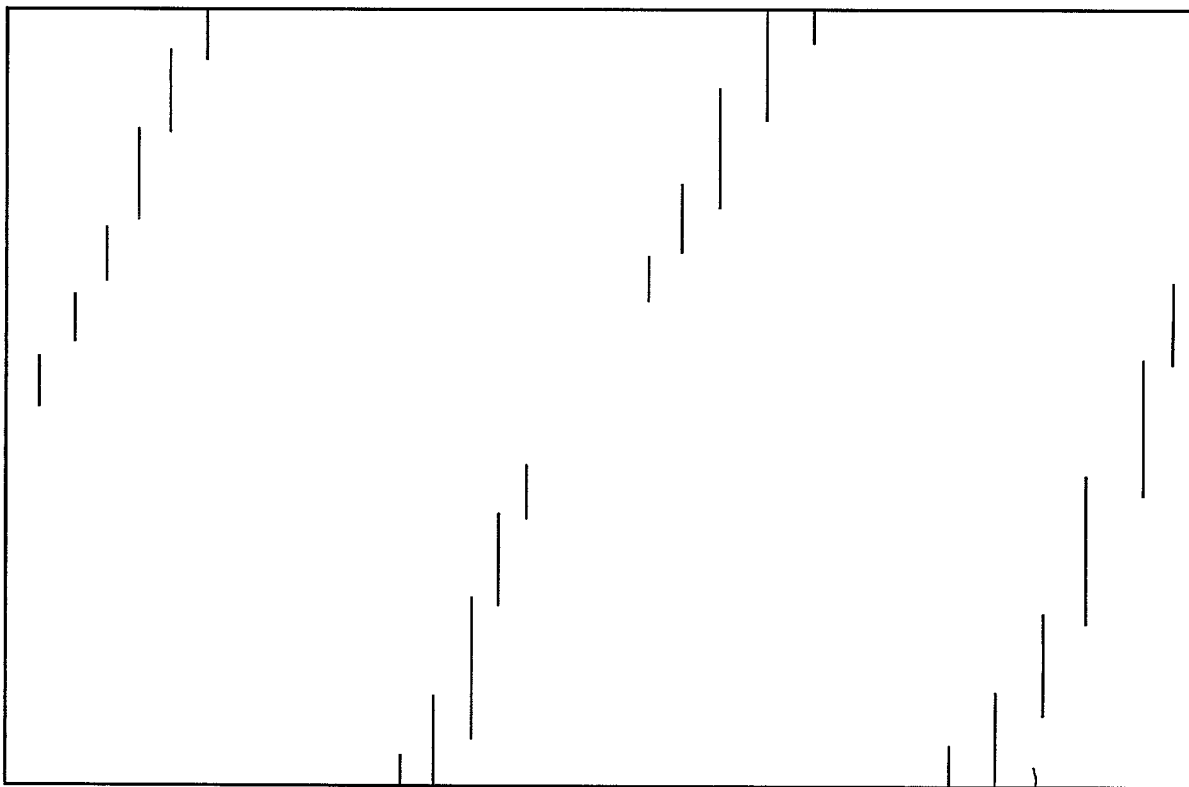
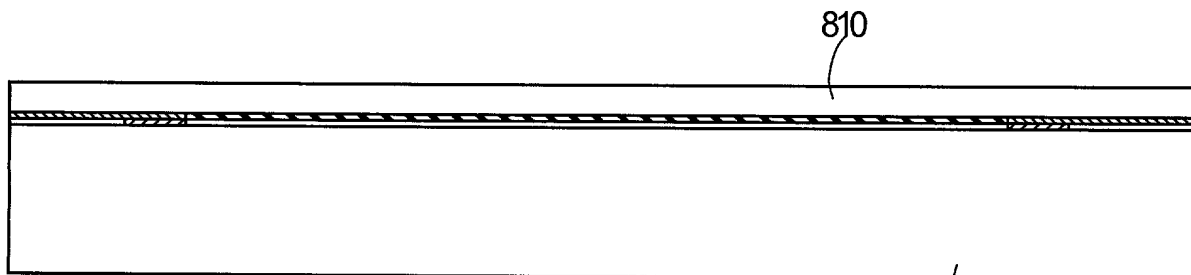


FIG. 7B



810

FIG 8A



310

FIG 8B

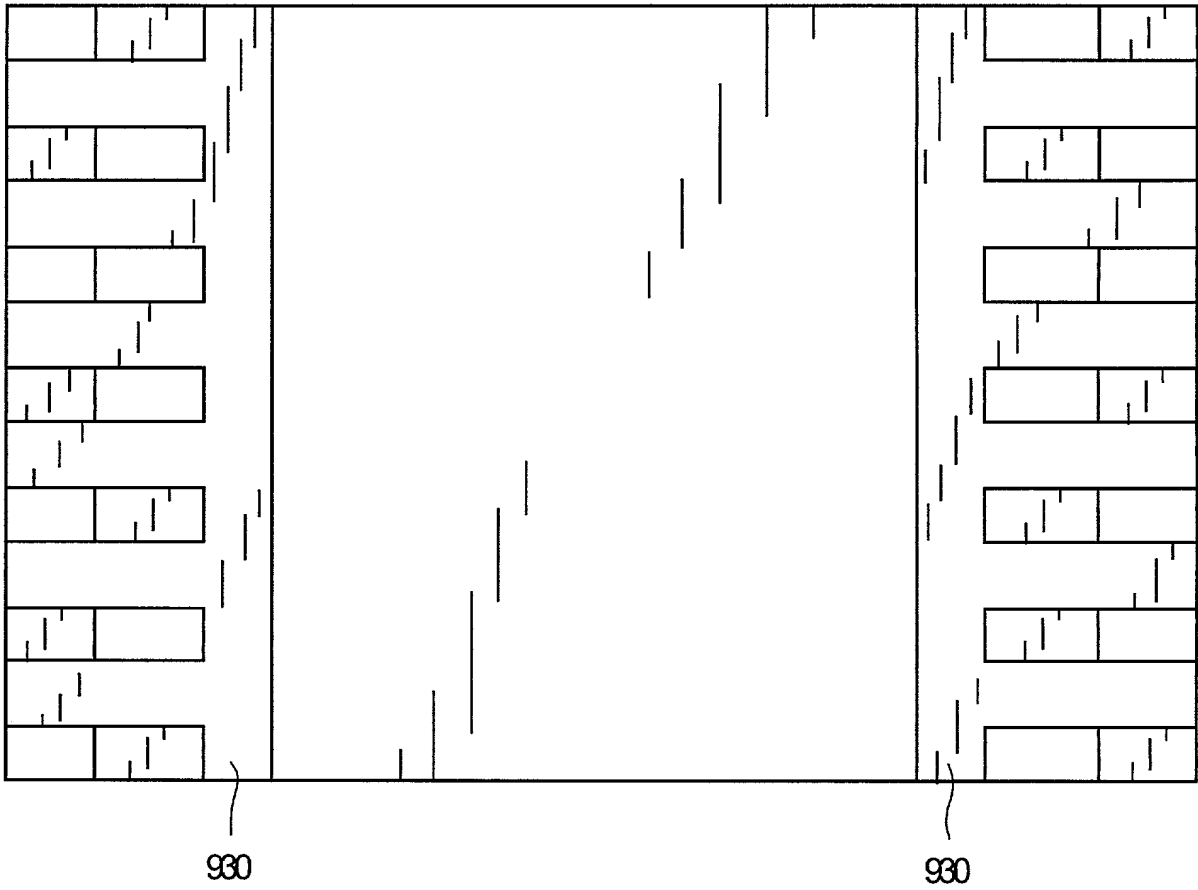


FIG. 9A

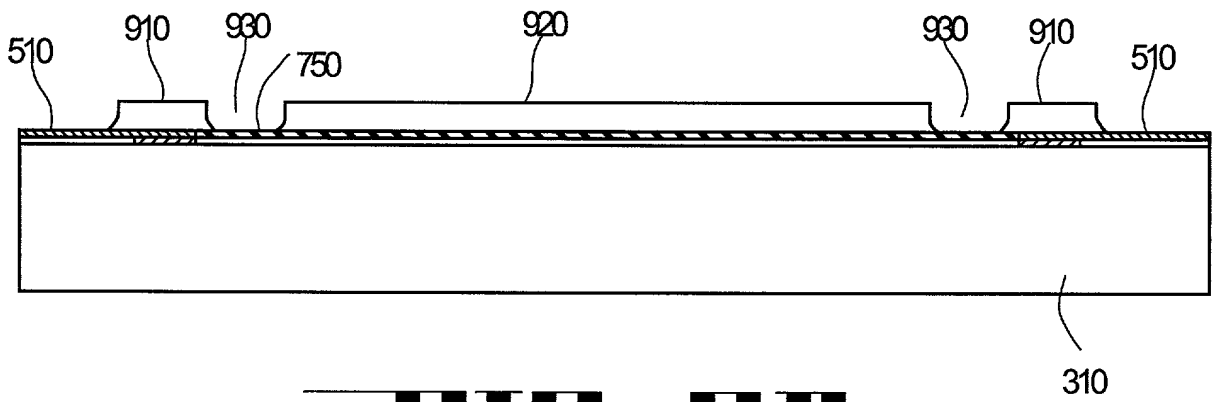


FIG. 9B

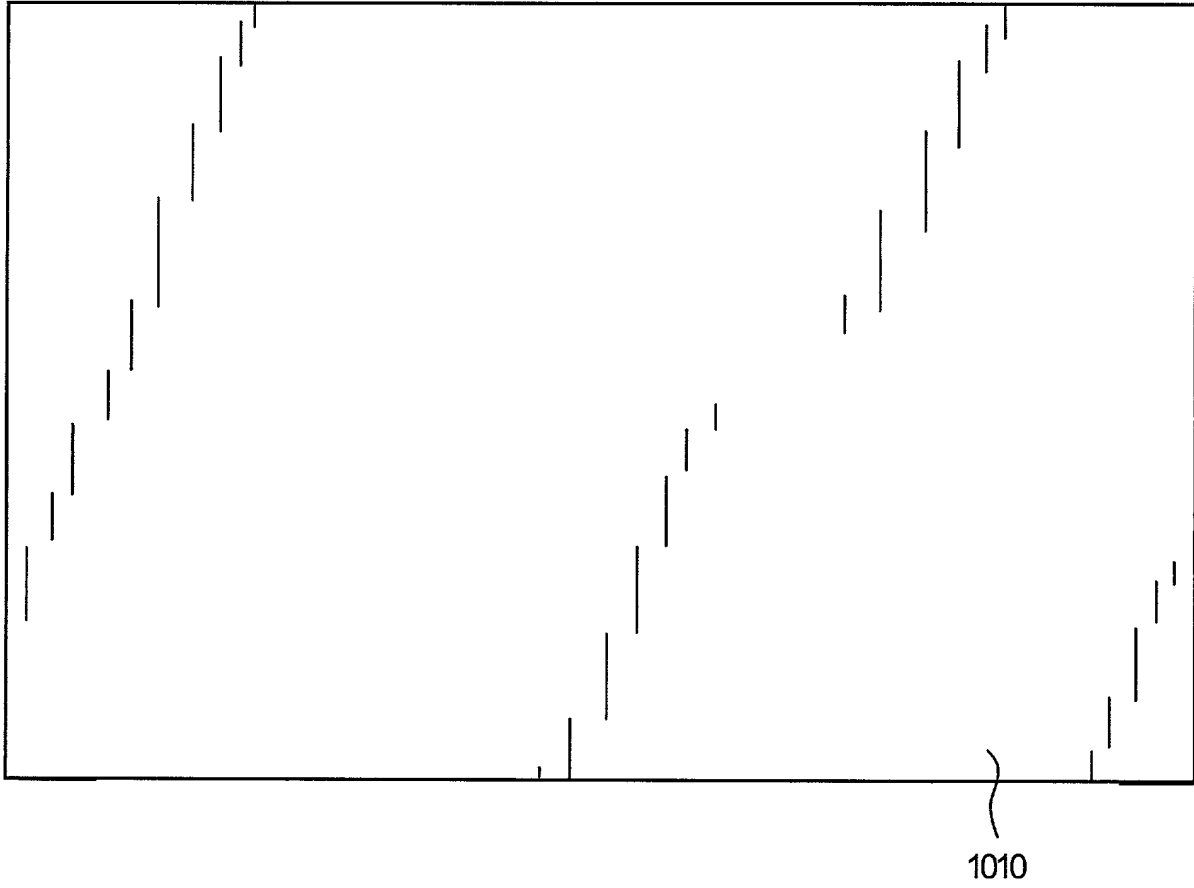


FIG. 10A

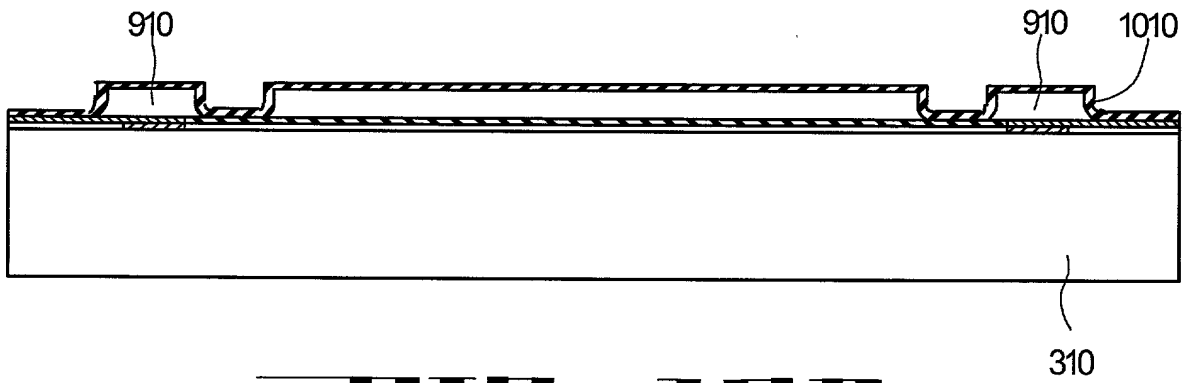


FIG. 10B

FIG. 11A is a schematic diagram of a device 1000 in a perspective view. The device 1000 includes a central region 1010 and two side regions 1110. The side regions 1110 are located on the left and right sides of the central region 1010. The side regions 1110 are defined by a series of rectangular blocks and lines, suggesting a complex, possibly multi-layered, structure. The central region 1010 is a large, empty rectangular area. The device 1000 is shown in a perspective view, with the central region 1010 and side regions 1110 being the primary components.

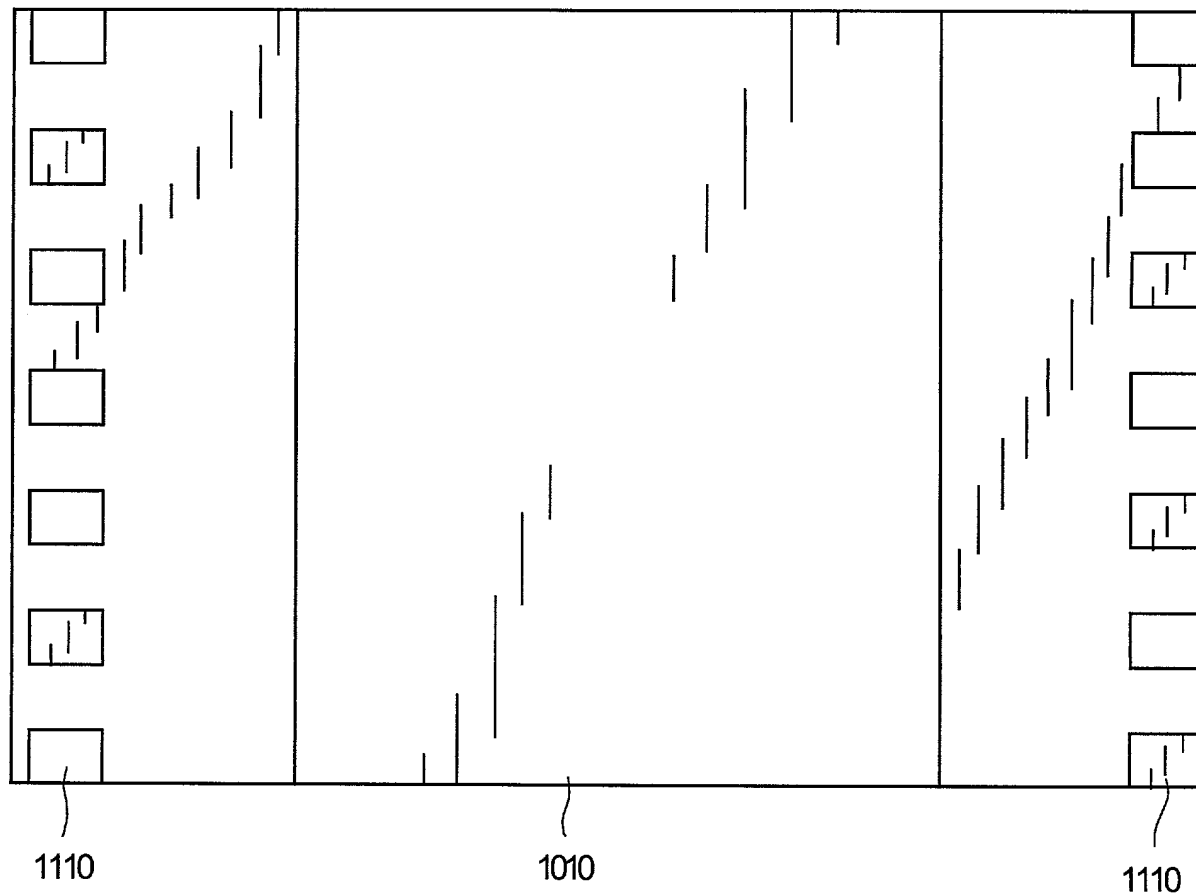


FIG. 11A

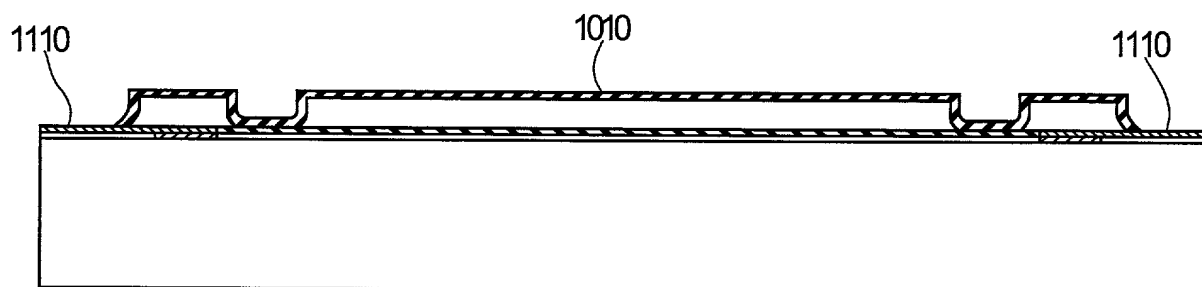
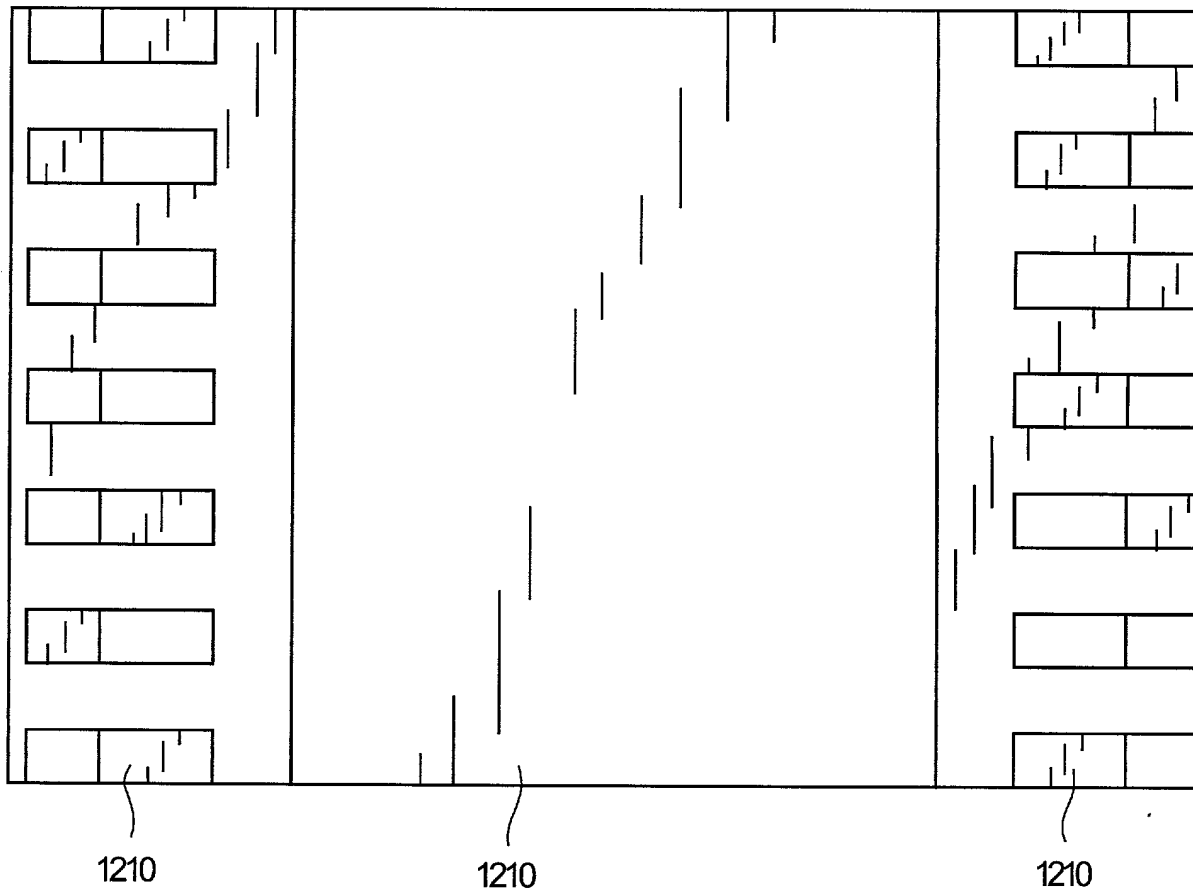
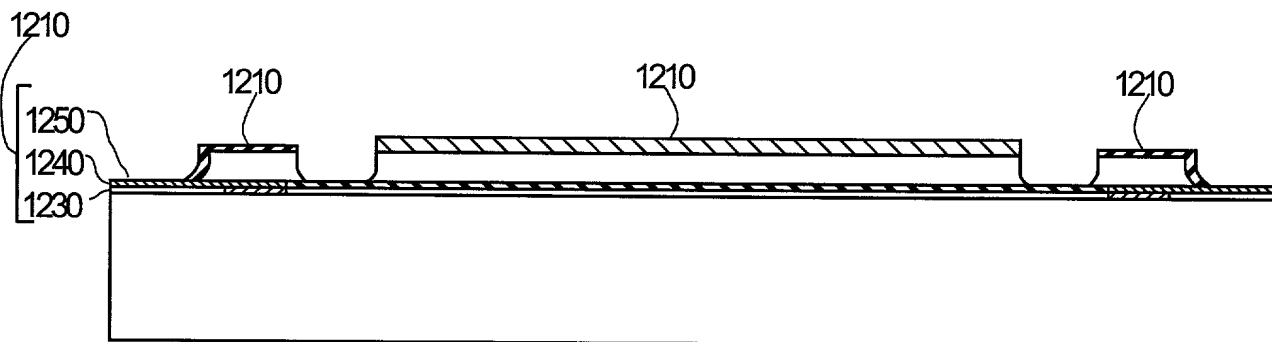


FIG. 11B

FIG. 12A is a top view of a device 1200. The device 1200 includes a central region 1210 and two side regions 1210. The side regions 1210 are located on the left and right sides of the central region 1210. The side regions 1210 are further divided into sub-regions 1210. The central region 1210 is further divided into sub-regions 1210. The device 1200 is shown in a perspective view.



FIG_12A



FIG_12B

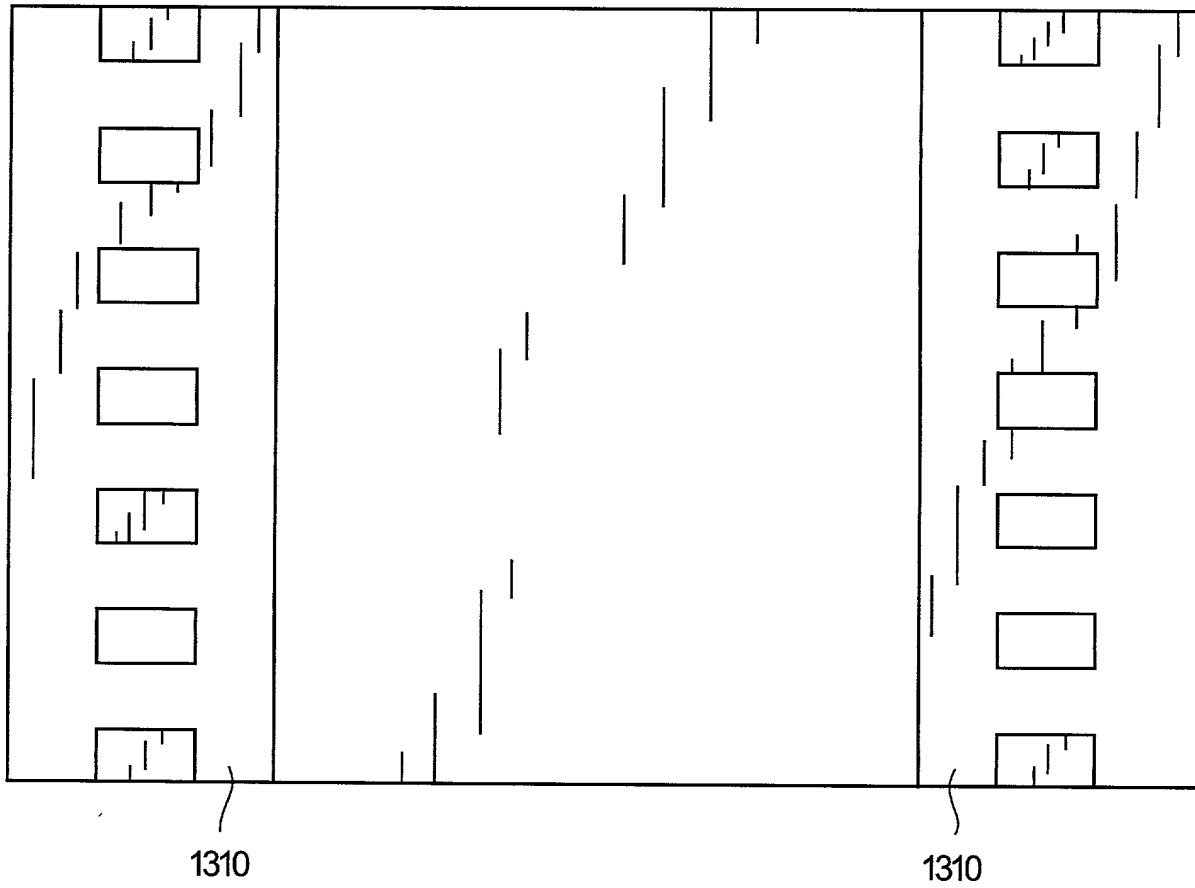


FIG 13A

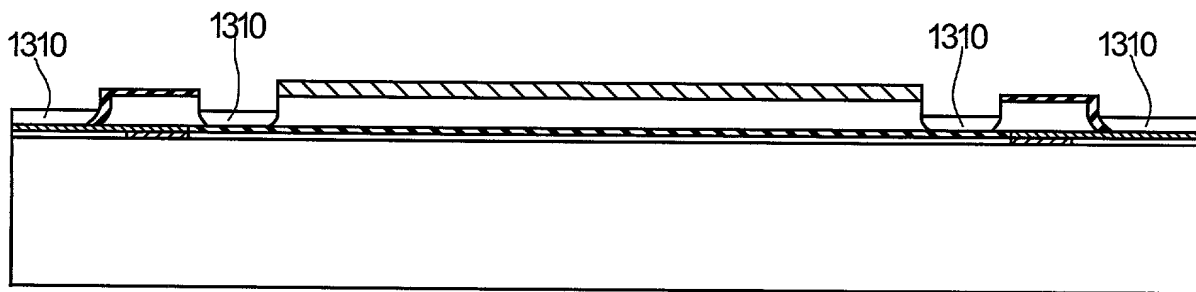


FIG 13B

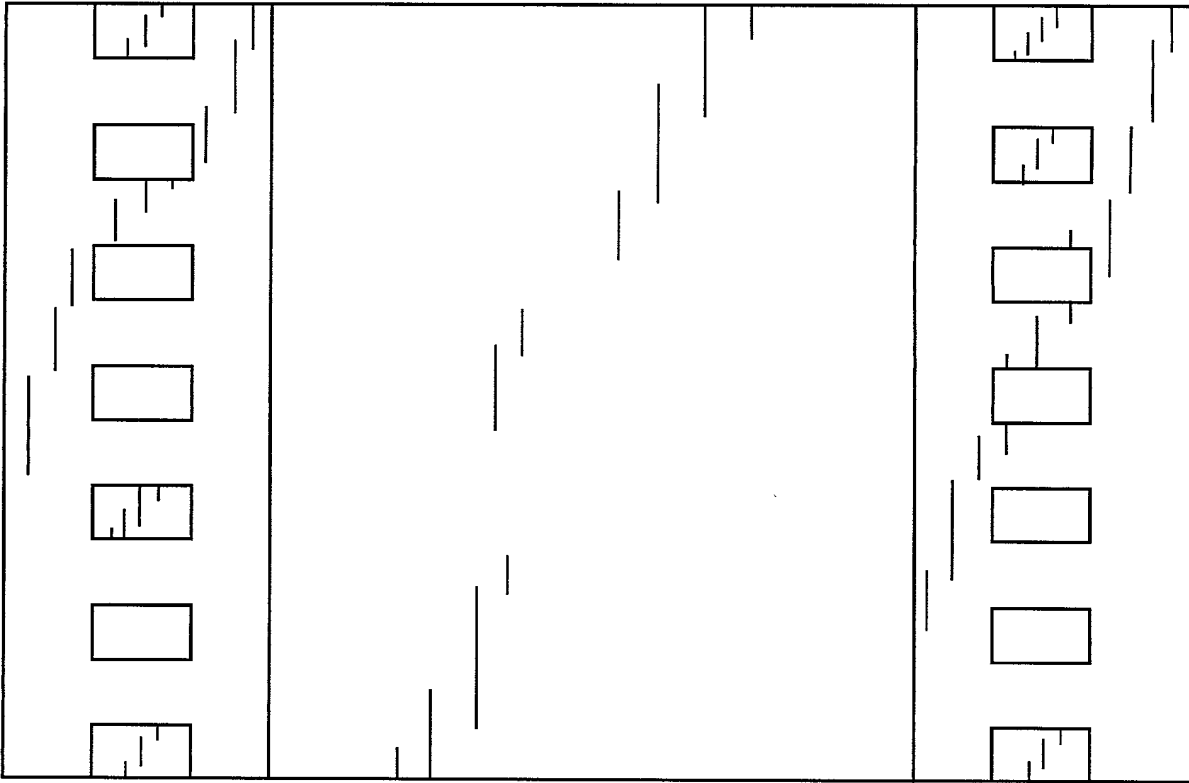
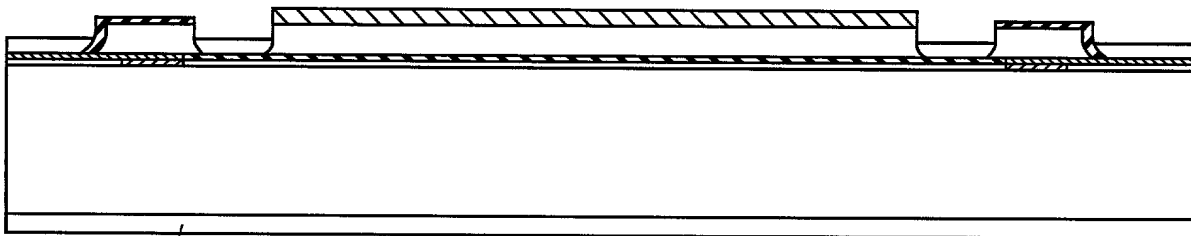


FIG 14A



1410

FIG 14B

FIG. 15A is a top view of a semiconductor device 1500. The device includes a central rectangular region 1580 and four smaller rectangular regions 1580 arranged in a 2x2 grid. The regions 1580 are separated by a material 1550. The device is mounted on a substrate 1560.

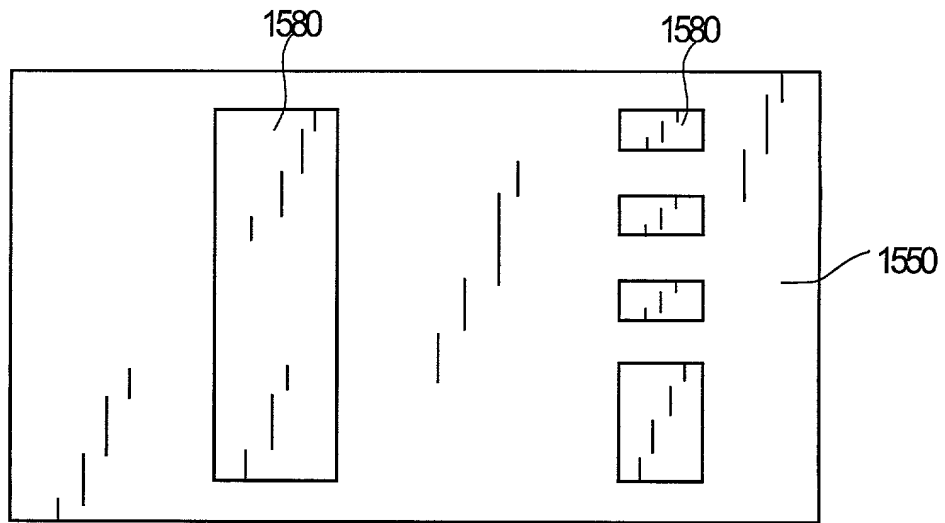


FIG. 15A

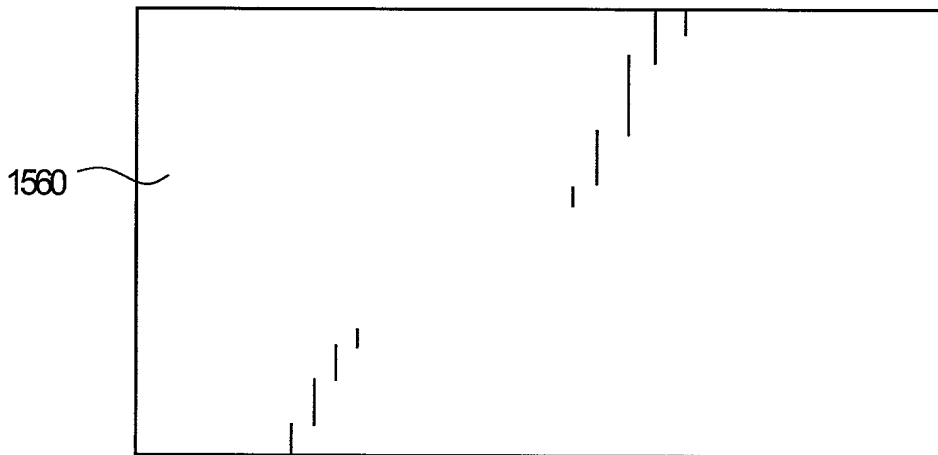


FIG. 15B

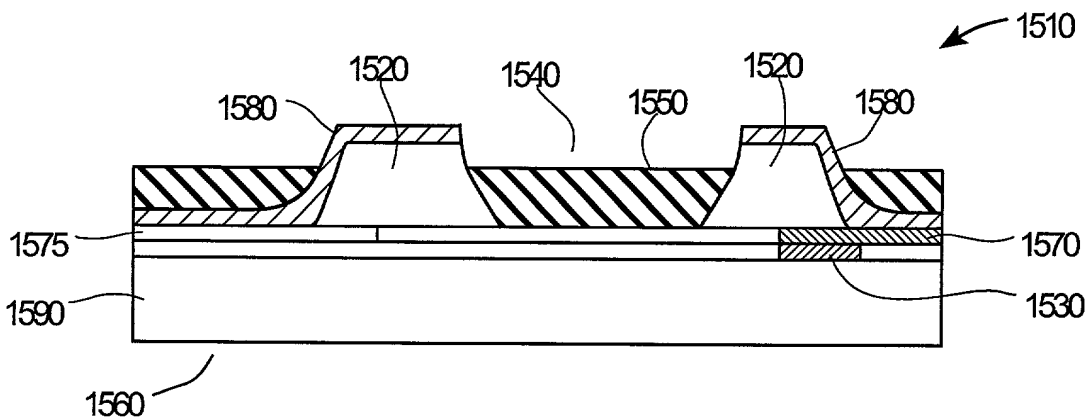


FIG. 15C

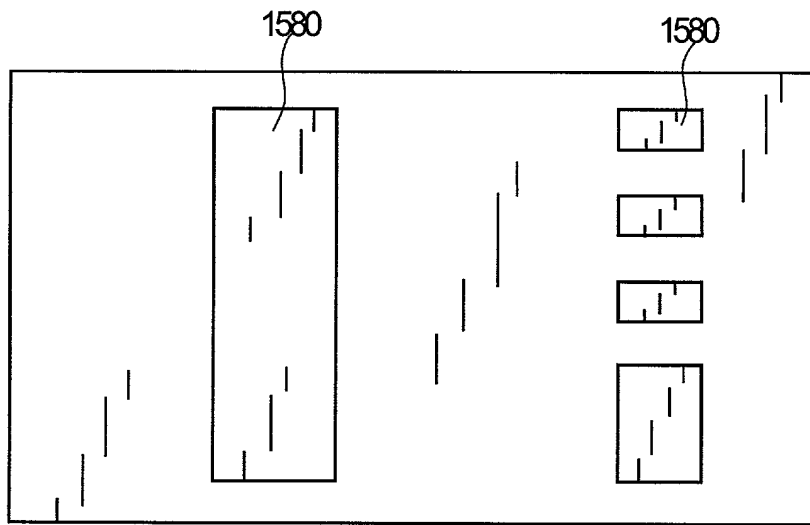


FIG 16A

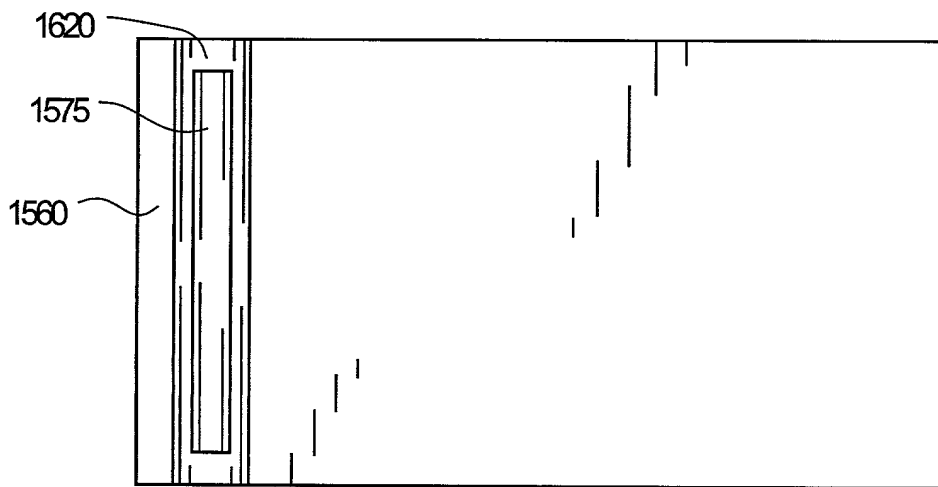


FIG 16B

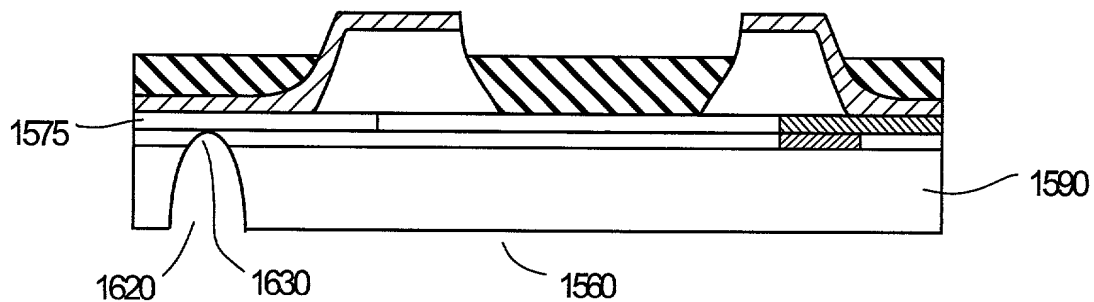


FIG 16C

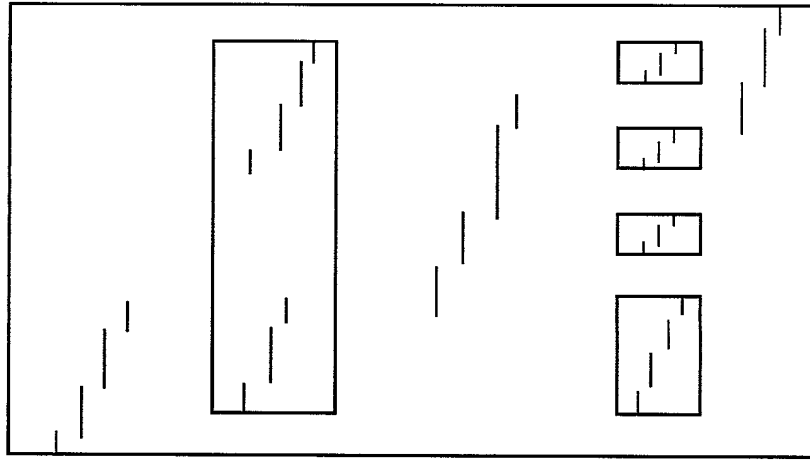


FIG 17A

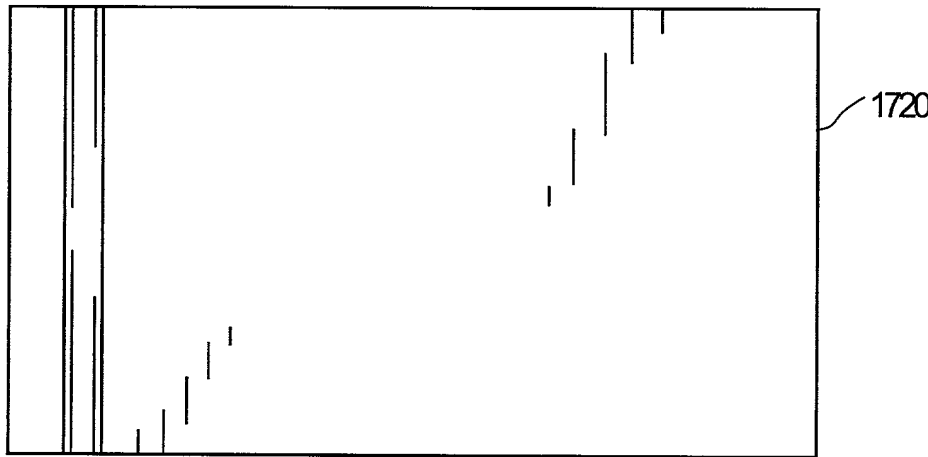


FIG 17B

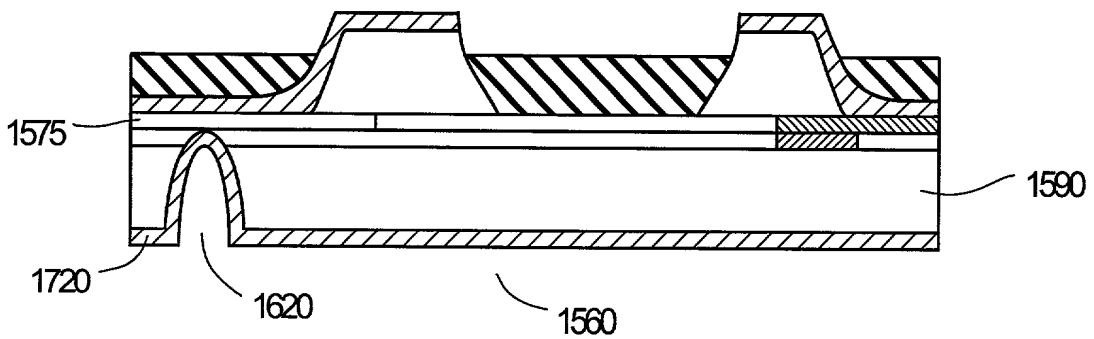


FIG 17C

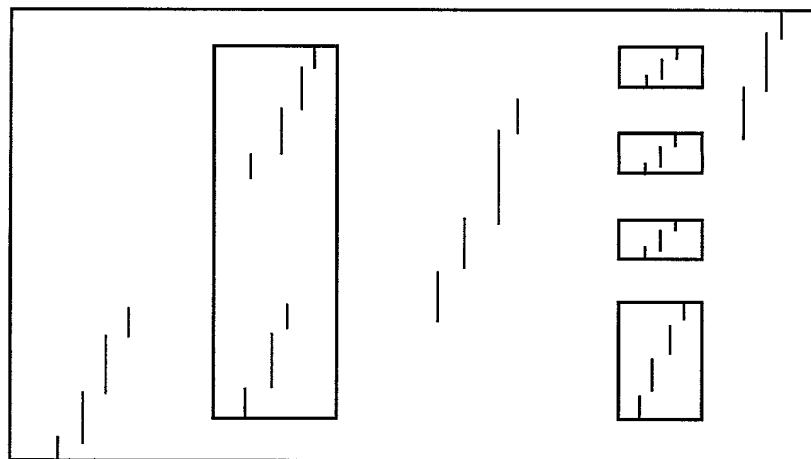


FIG 18A

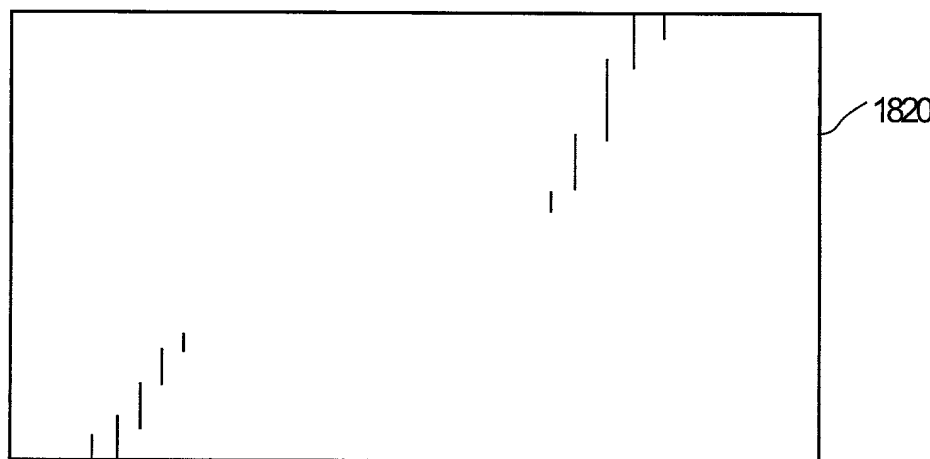


FIG 18B

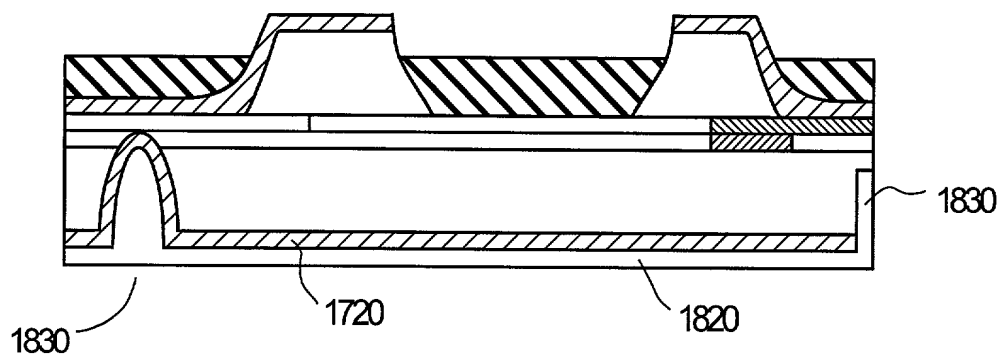


FIG 18C

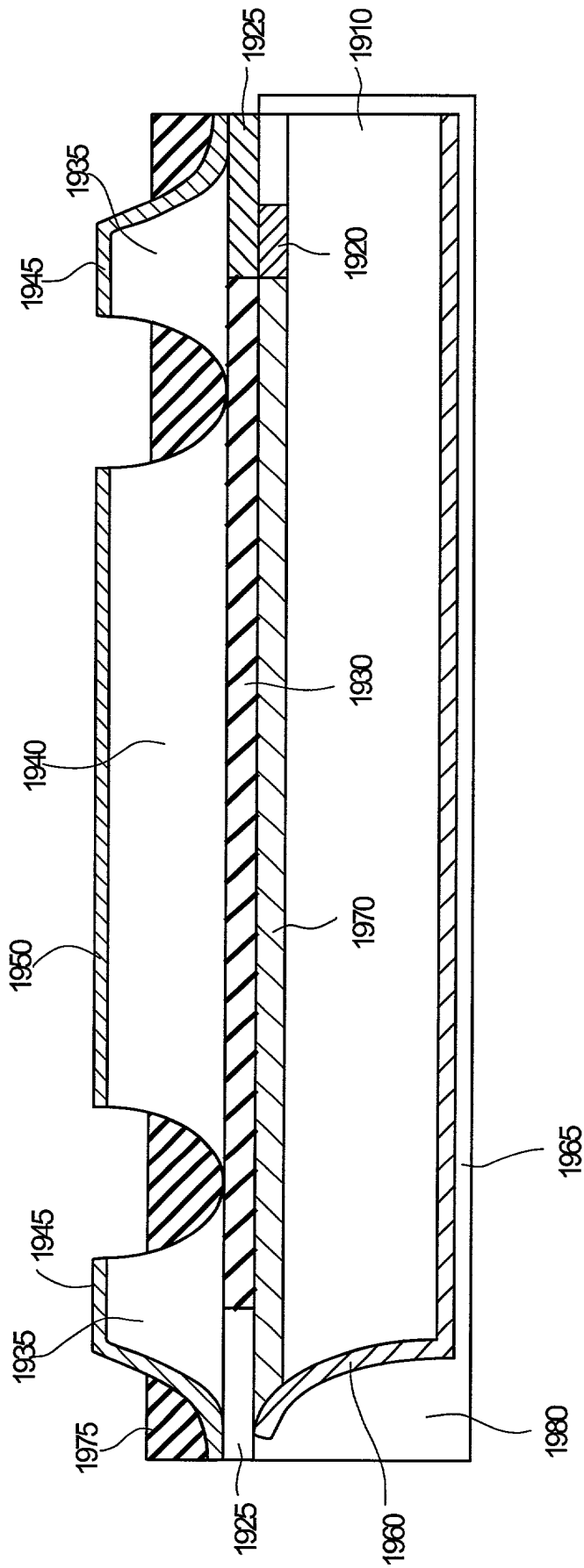


FIG. 19

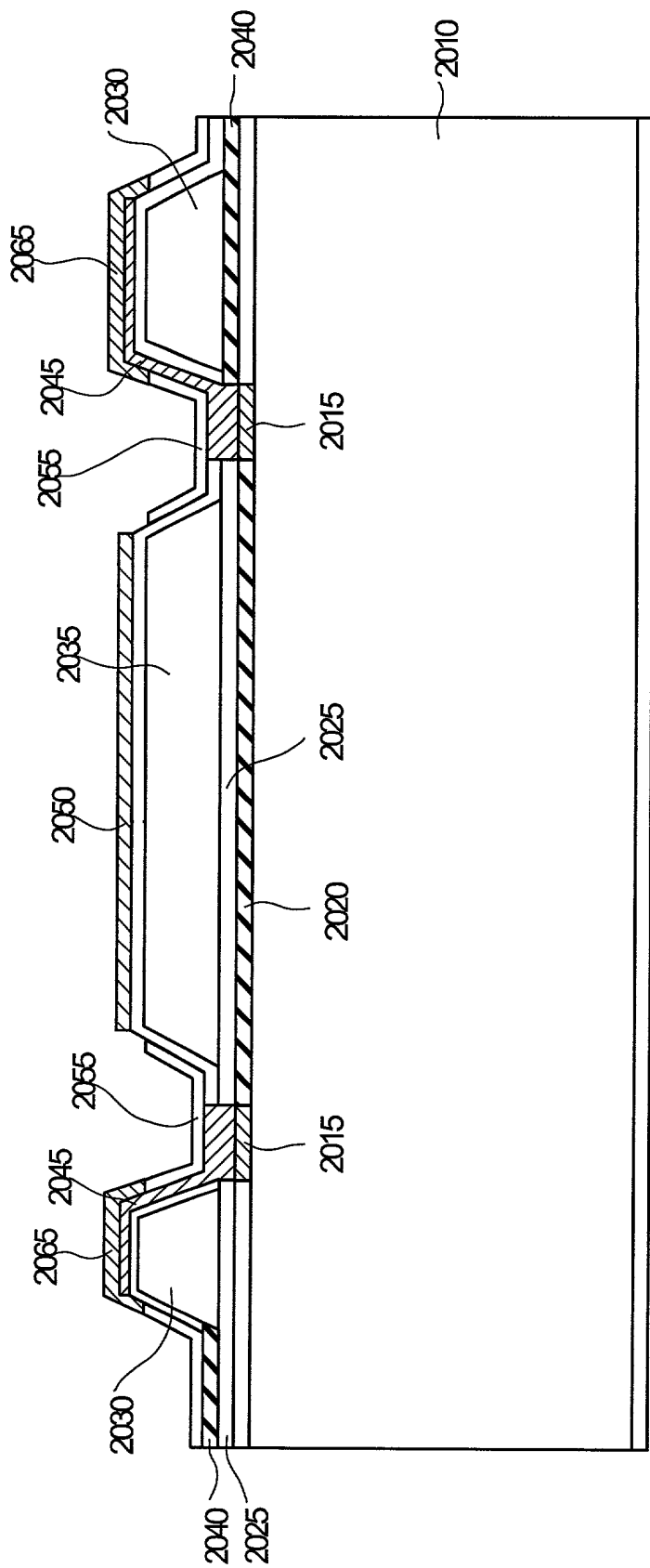
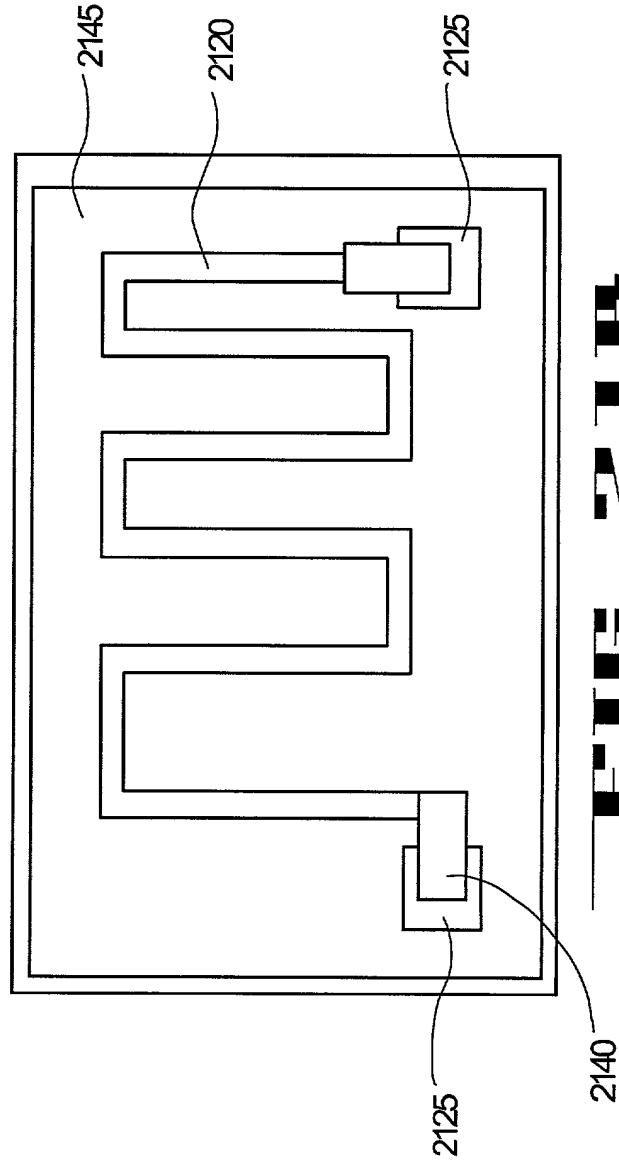
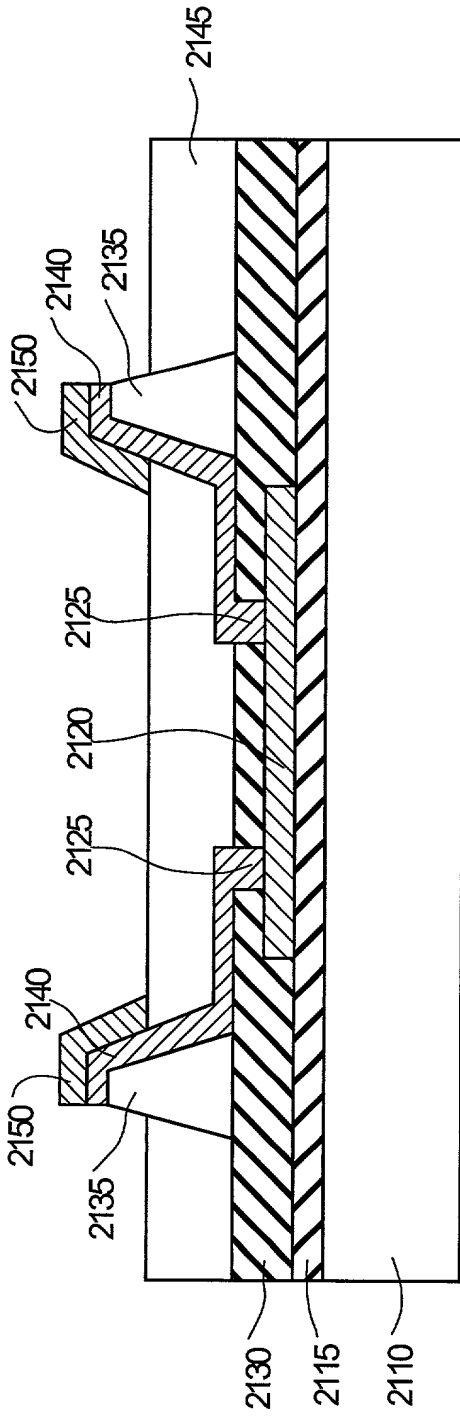


FIG. 20



ENTREPRENEUR

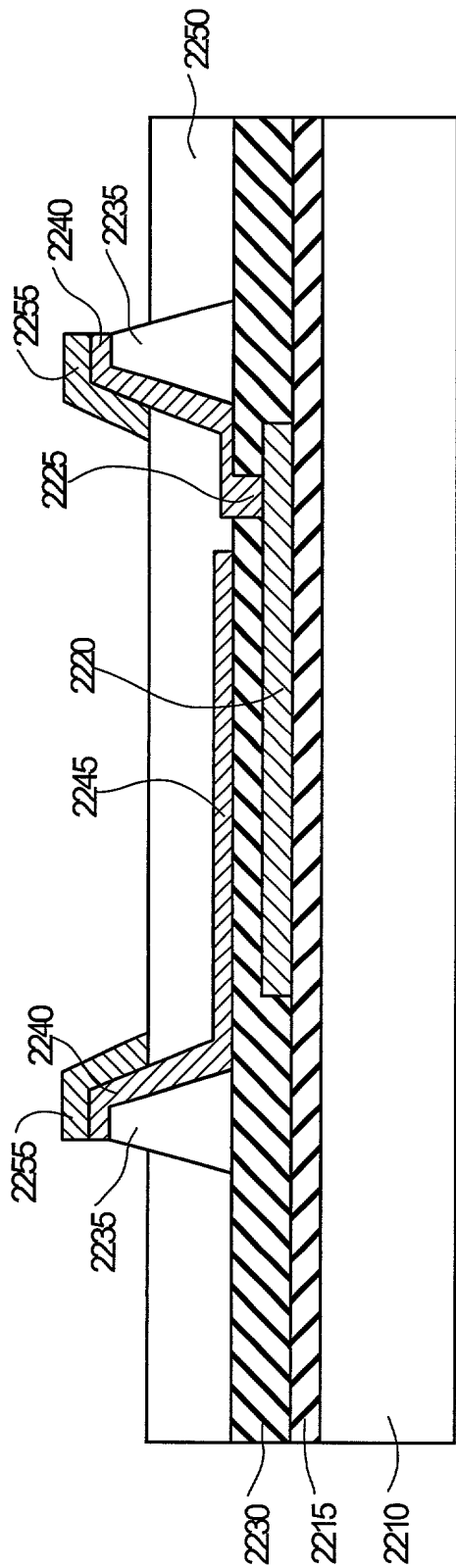


FIG. 22A

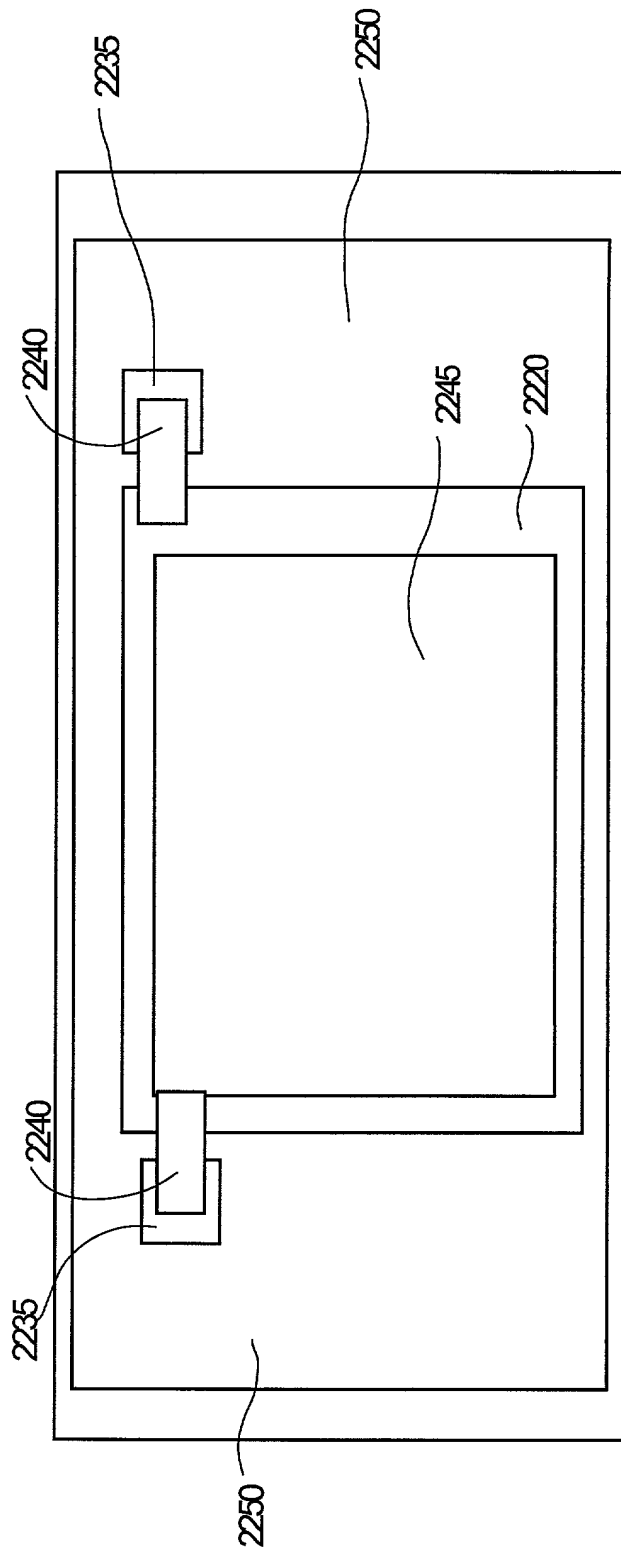


FIG. 22B

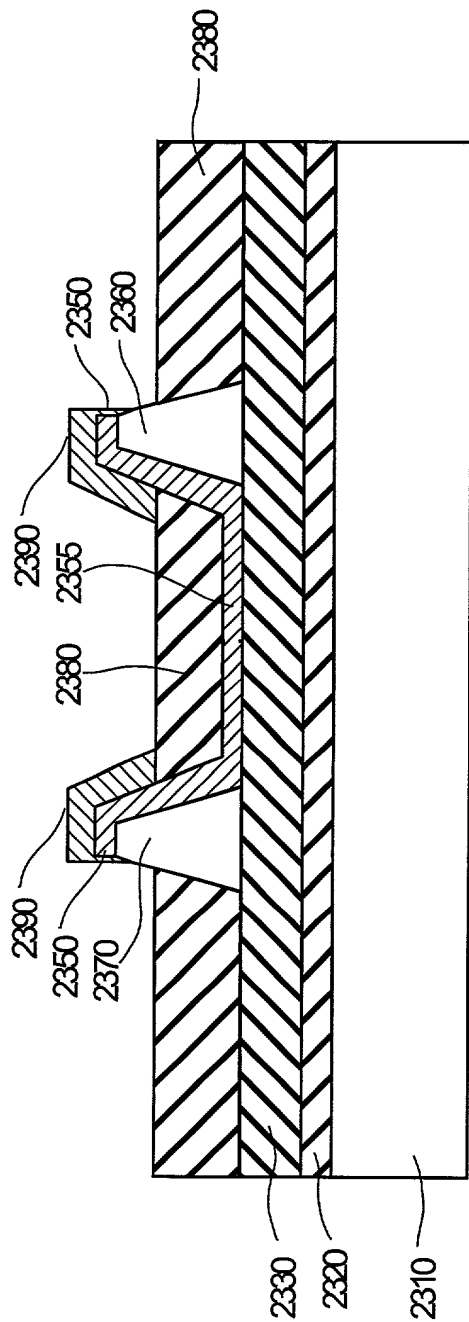


FIG. 23A

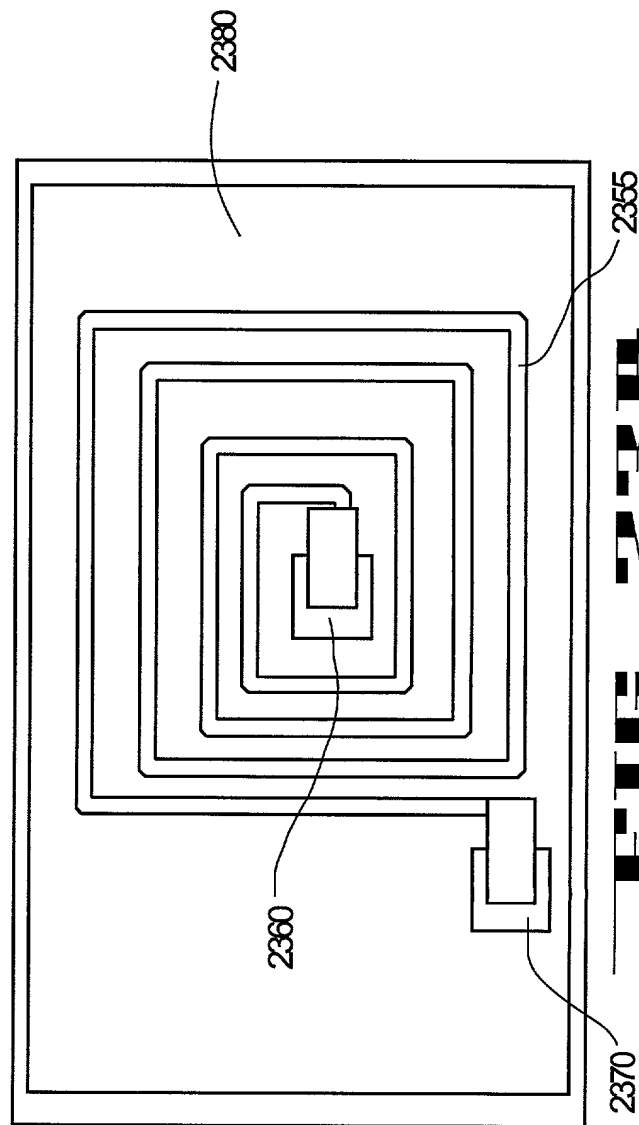


FIG. 23B

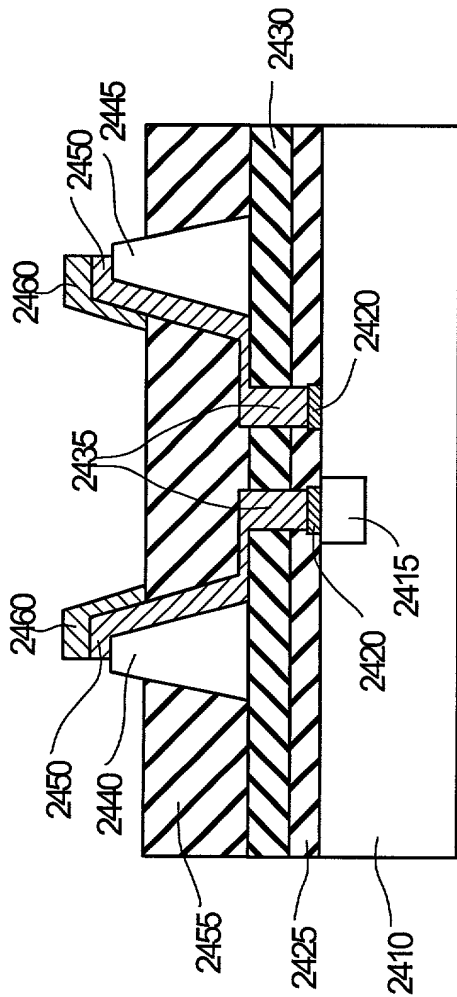


FIG. 24A

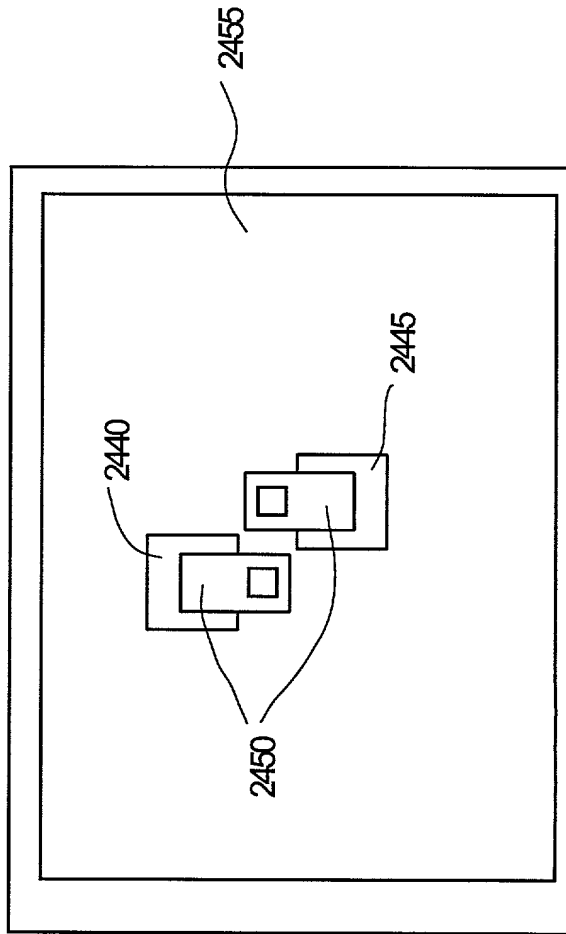


FIG. 24B